Test pitanja iz VHDL-a, 2021

1. Sta je pravo ime za VHDL?

a) Verilog Hardware Description Language

b) Very High speed Description Language

c) Variable Hardware Description Language

d) Very high speed Hardware Description Language

2. Koji je su od sledecih HDL jezika IEEE standardi?
a) VHDL i Verilog
b) C i C++
c) Altera i Xilinx
d) Quartus II i MaxPlus I

3. Sta je od donjeg karakteristika VHDL-a?
a) Case sensitive
b) Use of simple data types
c) Based on C programming language
d) Strongly typed language

4. Koje od sledecih blokova sadrzi osnovni VHDL program?
   a) Architecture
   b) Entity
   c) Process
   d) Package

5. Opis kola je dat u:
   a) Architecture
   b) Entity
   c) Library
   d) Configurations

6. Jedan entitet moze da sadrzi vise od 1-dne arhitekture?
a) True
b) False

7. U VHDL-u, Bus tip je?
a) Signal
b) Constant
c) Variable
d) Drive

8. Sta od sledeceg nije definisano u entitetu?
a) Direction of any signal
b) Names of signal
c) Different ports
d) Behavior of the signals

9. Sta od sledecega moze biti ime entiteta?
a) Nand_gate
b) NAND
c) AND
d) IF

10. Koja je od sledecih korektna sintaksa za deklaraciju entiteta?

a)

```
ENTITY entity_name IS
   PORT( signal_names : signal_modes;
   signal_names : signal_modes);
  END entity_name;
```

b)

```
 ENTITY entity_name
   PORT( signal_names : signal_modes;
   signal_names : signal_modes);
  END ENTITY
```

11. Sta je tacna deklaracija i definicija arhitekture?

a)

```
ARCHITECTURE architecture_type OF entity_name IS
    Declarations_for_architecture;
    BEGIN
    Code;
    ....
   END architecture_name;
```

b)

```
ARCHITECTURE architecture_name OF entity_name IS
    BEGIN
    Declarations_for_architecture;
    Code;
```

```
    ....
  END architecture_name;
```

c)

```
ARCHITECTURE architecture_type OF entity_name IS
   BEGIN
   Declarations_for_architecture;
   Code;
   ....
  END architecture_type;


ARCHITECTURE architecture_name OF entity_name IS
   Declarations_for_architecture
   BEGIN
   Code;
   ....
   END architecture_name;
```

12. SIGNED i UNSIGNED data tipovi su definisani u?
    a) std_logic_1164 package
    b) std_logic package
    c) std_logic_arith package
    d) standard package

13. Koju vrijednost poprima x u sledecem kodu?

```
SIGNAL x : IN UNSIGNED (3 DOWNTO 0 );
x <= "1100";
```

a) 12
b) 5
c) -5
d) 14

14. SIGNAL a : REAL; sta je od donjeg nedozvoljeno pridruzivanje za a)?

a) a <= 1.8
b) a <= 1.0 E10
c) a <= 1.0 E-10
d) a <=1.0 ns

15. Vise dimenzionalni nizovi se mogu upotrijebiti za implementaciju memorije?

a) True.
b) False.

16. Sta od sledeceg ne moze biti vrijednost za x? Pogledaj donji kod?

```
TYPE color IS (red, green, blue, black, white, gray);
SUBTYPE primary IS color RANGE red to blue;
VARIABLE x: primary;
```

a) White
b) Red
c) Green
d) Blue

17. Koliko bitova moze biti smjesteno u promenljivu array2

```
TYPE array1 IS ARRAY ( 0 TO 3 ) OF BIT_VECTOR (3 DOWNTO 0 );
TYPE array2 IS ARRAY ( 0 TO 3 ) OF array1;
```

a) 16
b) 9
c) 64
d) 27

18. Korisnik moze definisati svoj integer tip?

a) True
b) False

19. U VHDL mozete primijeniti osnovne aritmeticke operacije nad razlicitim tipovima podataka?
    a) True
    b) False

20. U donjem kodu sta ce biti greska pri kompalaciji?

```
TYPE my_int IS INTEGER RANGE -32 TO 32;
TYPE other_int IS INTEGER RANGE 0 TO 100;
SIGNAL x : my_int;
SIGNAL y : other_int;
y <= x + 2;
…
```

a) Type mismatch
b) Syntax problem
c) No declaration
d) Can’t compile

21. Kojeg tip ce biti vrijednost y poslije izvrsavanja sledeceg koda, koliko bita?

```
Library ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
…
SIGNAL m : UNSIGNED (3 DOWNTO 0);
SIGNAL n : UNSIGNED (3 DOWNTO 0);
SIGNAL y : STD_LOGIC_VECTOR (7 DOWNTO 0);
y <=CONV_STD_LOGIC_VECTOR ((m+n), 8);
…
```

a) 8- bit STD_LOGIC_VECTOR m+n
b) 8- bit UNSIGNED m+n
c) 4- bit STD_LOGIC m+n
d) Error

22. Koji od donjih operatora nije operator pridruzivanja?
a) <=
b) :=
c) =>
d) =

23. A VARIABLE y je deklarisana kao STD_LOGIC_VECTOR tip, 4 bita, ako zelis da pridruzis 1001 za y, koji je pravi izraz ?
a) y <= "1001"
b) y := "1001"
c) y <= '1', '0', '0', '1'
d) y => "1001"

24. Sta je funkcija shift operatora?
a) To shift the data
b) To shift the identifiers
c) To shift the operators
d) To shift the STD_LOGIC_VECTOR

25. a <= b after 10ns; u ovoj recenici se definise delay?
a) True
b) False

26. Koje je kolo definisano donjim kodom?

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;
ENTITY my_func IS
PORT(x, a, b : IN std_logic;
q : OUT std_logic);
END my_func;
ARCHITECTURE behavior OF my_func IS
SIGNAL s : INTEGER;
BEGIN
WITH s SELECT
q <= a AFTER 10 ns WHEN 0;
       b AFTER 10 ns WHEN 1;
s <= 0 WHEN x = '0' ELSE
      1 WHEN x = '1';
END behavior;
```

a) AND gate
b) OR gate
c) MUX 2:1
d) DEMUX 1:2

27. U kojem dijelu VHDL koda se definise generic, dati primjer?
a) Package declaration
b) Entity
c) Architecture
d) Configurations

28. Ako postoji vise procesa u VHDL kodu kako se oni izvrsavaju?
a) One after the other
b) Concurrently
c) According to sensitivity list
d) Sequentially

29. Local varijable u procesu mogu biti definisane na kojem mjestu?
a) Anywhere within the process
b) After a sequential statement
c) Before the BEGIN keyword
d) After the BEGIN keyword

30. Koja je o donjih ispravna sintaksa za deklaraciju procesa ?

a)

```
{Label :} PROCESS
{process_declaration_part};
 sensitivity_list;
BEGIN
sequential_statements;
END PROCESS {Label};
```

b)

```
PROCESS {sensitivity_list}
{process_declaration_part}
BEGIN
sequential_statements;
END PROCESS {Label};
```

c)

```
{Label :} PROCESS
{process_declaration_part}
BEGIN
sensitivity_list;
sequential_statements;
END PROCESS;
```

d)

```
{Label :} PROCESS {sensitivity_list}
{process_declaration_part}
```

```
BEGIN
sequential_statements;
END PROCESS {Label};
```

31. Koja od donjih kljucnih rijeci ne pripada If naredbi?
    a) ELSE
    b) THEN
    c) WHEN
    d) ELSIF

32. Koliko iteracija ce se odraditi u donjoj for petlji?

```
FOR i IN 0 TO 5 LOOP
```

a) 6
b) 4
c) 5
d) 7

33. Koja je od donjih tacna upotreba signala?
a) To set default value
b) To declare a variable
c) To represent local information
d) To pass value between circuits

34. Koja je od donjih promenljivih lokalna za blok u kojem se deklarise?
a) Signal
b) Variable
c) Constant
d) Float

35. Konstanta koja je definisana u ARCHITECTURE, bice dostupna

a) In the process within the architecture
b) Whole code
c) Within the same architecture
d) In the entity associated and corresponding architecture

36. U procesu se dodjeljuje variabla, nova vrijednost se dodjeljuje
a) After one delta cycle
b) Immediately
c) At the end of a process
d) At the end of architecture

37. Ne postoji delay u slucaju varijabli
a) True
b) False

38. Sta je tacno u vezi package?
a) Package is collection of libraries
b) Library is collection of packages
c) Package is collection of entities
d) Entity is collection of packages

e) Package is collection of the components

39. Ono sto je deklarisano u package je vidljivo za:
a) Every design unit
b) Package body only
c) Library containing that package
d) Design unit that USE the package

40. Koji je standardni package ukljucen u VHDL kod i ne mora se deklarisati?

a) STD_LOGIC_1164

b) STANDARD
c) TEXTIO
d) STD_LOGIC_ARITH

41. Funkcija se poziva iz:
a) Function itself
b) Library
c) Main code
d) Package

42. Koliko vracenih vrijednosti posjeduje funkcija?
a) 1
b) 2
c) 3
d) 4

43. Da li funkcija u VHDLu moze imati imati vise parametara

a) False

b) True

44. Sta od sledeceg moze biti parameter funkcije?

```
SIGNAL a, b : IN STD_LOGIC
VARIABLE c : INTEGER
CONSTANT d : INTEGER
```

a) a
b) a,b
c) a,b,c
d) d

45. Kakve direkcije je signal kao argument donje funkcije?

```
FUNCTION my_func (SIGNAL a : STD_LOGIC_VECTOR) RETURN INTEGER IS
…..;
```

a) IN
b) OUT
c) INOUT
d) BUFFER

46. Procedura u VHDL-u vraca vrijednos?

a) False
b) True

47. Sta ce da bude vrijednost sekvence my_array'LENGTH, ako je definisana na sledeci nacin?

```
TYPE my_array IS ARRAY (15 DOWNTO 0) OF STD_LOGIC;
```

a) 15
b) 8
c) 0
d) 16

48. Sekvenca atributa definisana dolje opisuje stanje kloka:

```
IF (clk'EVENT and clk = '1')
```

a) Rising edge of the clock signal
b) Falling edge of the clock signal
c) Clock signal frequency
d) Time period of clock signal

49. Koje je logicko kolo opisano donjim kodom?

```
ARCHITECTURE gate OF my_gate IS
BEGIN
WITH ab SELECT
y<= 0 WHEN "01" OR "10";
     1 WHEN OTHERS;
END gate;
```

a) NAND
b) NOR
c) EXOR
d) EXNOR

50. Koji se od donjih atributa primenjuju u sekvencijalnim kolima?

a) 'STABLE
b) 'LENGTH
c) 'LAST_EVENT
d) 'EVENT