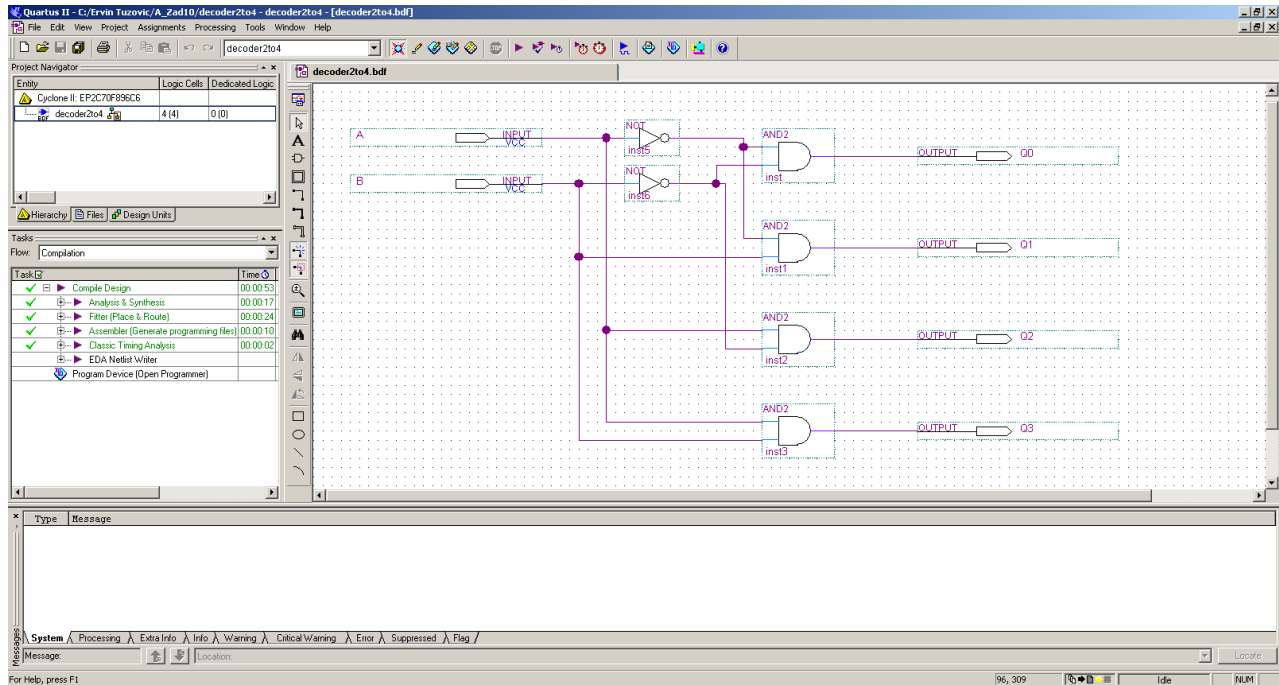


# Rešenje student Ervin Tuzović, 42/19

Zadaci: 1. A\_dio\_10 zadatak  
2. B\_dio\_3 zadatak

6+0+6+0=12/30

## 1. Block diagram:

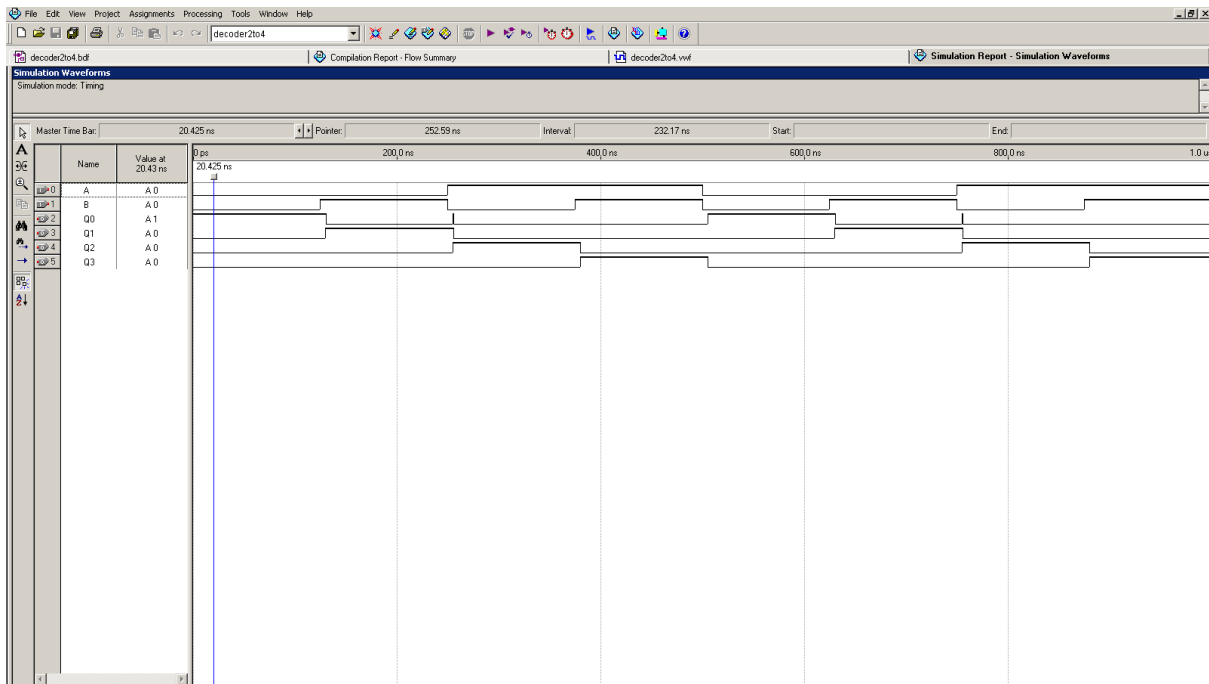


## Report:

Flow Status	Successful - Tue Apr 07 17:19:51 2020
Quartus II Version	9.1 Build 222/10/21/2009 SJ Web Edition
Revision Name	decoder2to4
Top-level Entity Name	decoder2to4
Family	Cyclone II
Device	EP2K10K10-10
Timing Models	Final
Met timing requirements	Yes
Total logic elements	4 / 68,416 (< 1 %)
Total combinational functions	4 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	6 / 522 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Info: Assembler is generating device programming files  
Info: Quartus II Assembler was successful. 0 errors, 0 warnings  
Info: \*\*\*\*\*  
Info: Running Quartus II Classic Timing Analyzer  
Info: Command: quartus\_tan --read\_settings\_files=off --write\_settings\_files=off decoder2to4 -c decoder2to4 --timing\_analysis\_only  
Info: Longest tpd from source pin "A" to destination pin "Q0" is 5.649 ns  
Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings  
Info: Quartus II Full Compilation was successful. 0 errors, 4 warnings

## Simulacioni dijagram:



**15** (-3 simulacioni diagrami nijesu objasnjeni)/2=**6**  
**ZA A=0, B=0, D0=1, D1=0, D2=0, D3=0;**

### 2. Kod:

```
library ieee ;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_unsigned.all;
```

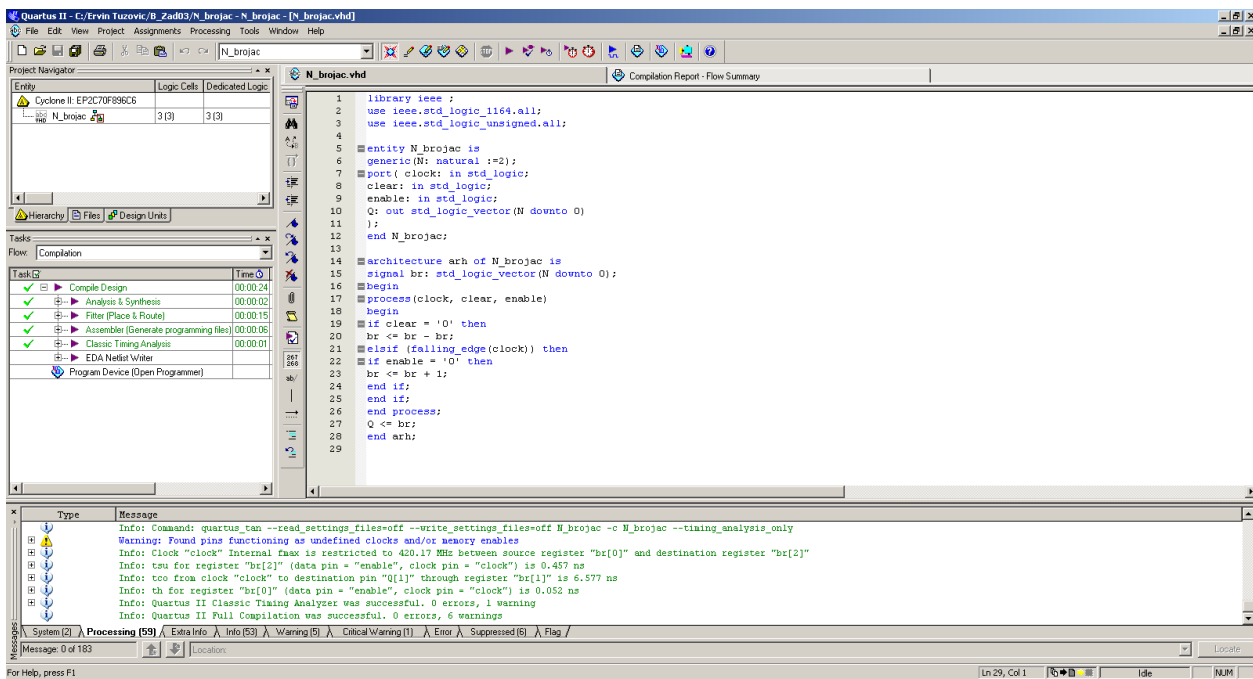
```
entity N_brojac is  
generic (N: natural :=2);  
port  
(  
    clock: in std_logic;  
    clear: in std_logic;  
    enable: in std_logic;  
    Q: out std_logic_vector (N downto 0)  
);  
end N_brojac;
```

```
architecture arh of N_brojac is  
signal br: std_logic_vector (N downto 0);  
begin
```

```

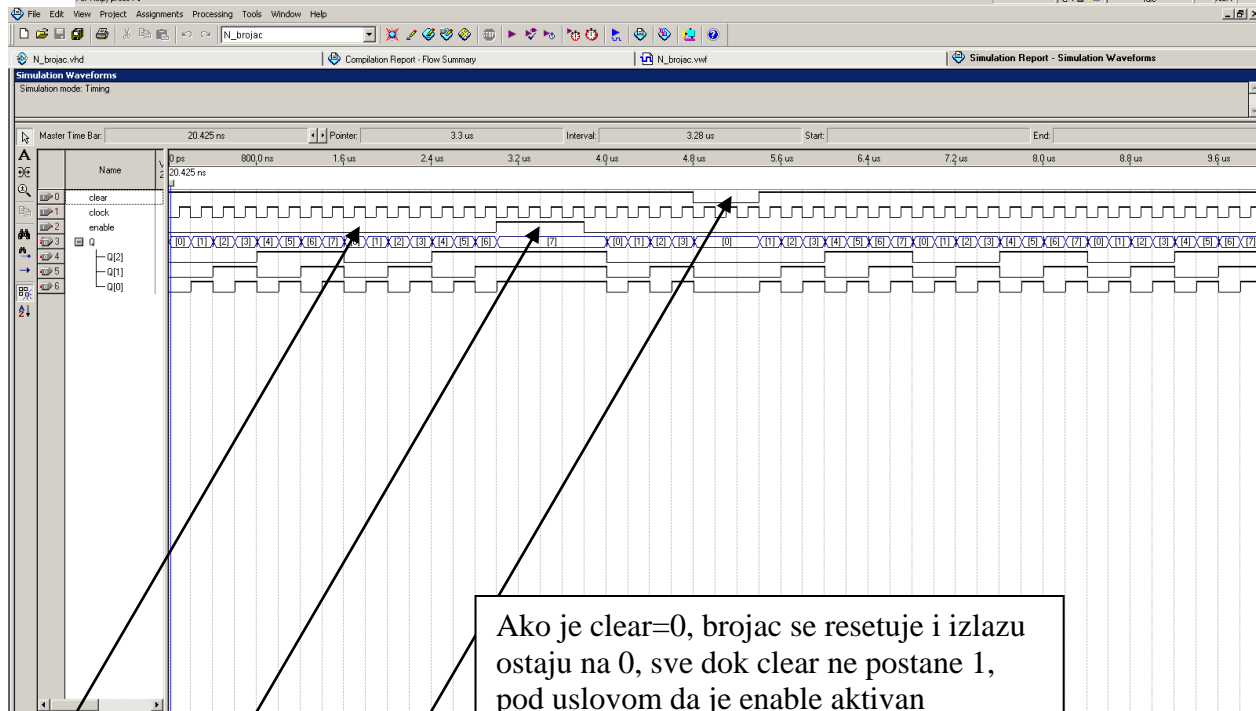
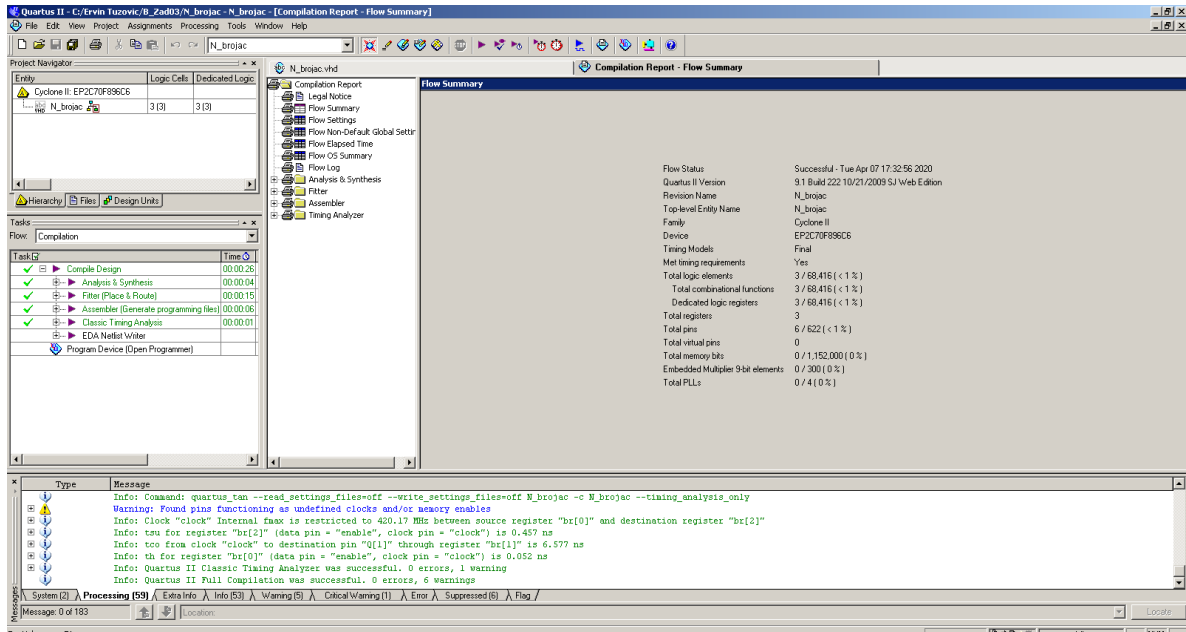
process (clock, clear, enable)
begin
    if clear = '0' then
        br <= br - br;
    elsif (falling_edge (clock)) then
        if enable = '0' then
            br <= br + 1;
        end if;
    end if;
end process;
Q <= br;
end arh;

```



**Report:**

# Simulacioni dijagram



Ako je clear=0, brojac se resetuje i izlazu ostaju na 0, sve dok clear ne postane 1, pod uslovom da je enable aktivan

Ako je enable=1, brojac ne broji, vec zadržava trenutnu vrijednost

Ako je clear=1 i enable=0, brojac broji od 0 do 7 na silaznu ivicu clocka