Appendix C: DE2 Pin Assignments

The most commonly used DE2 pin assignments are given in tables that follow, both for the standard DE2 board (with the EP2C35 FPGA) and the DE2-70 (with the EP2C70 FPGA).

If the vector names are used in your designs, you should create a pin for every lower-subscripted pin of that same type. For example, if you use the pin LEDR[3], you should also create pins for LEDR[0], LEDR[1], and LEDR[2]. In this case of LEDs, the extra pins might be tied to a GND symbol to keep the LEDs unlit. Alternatively, you could create different names that are not vector members.

One advantage of using the exact names given here, though, is that you can save yourself the effort of manually entering pin assignments in the Pin Planner. If you use the names in the tables, you can download a file called DE2_PINS.QSF (or DE2_70_PINS.QSF for the DE2-70) from the course web site. Then, you can import all pin assignments by selecting **Assignments => Import Assignments. . .** and then choose the downloaded file as the import source file. Verify in the Pin Planner that all pins have assignments after the import.

Note that the GPIO pins have been given the same names used by the board manufacturer, in order to be consistent. Unfortunately, there are two confusing aspects to their naming system:

- GPIO_0 pins are on JP1, while GPIO_1 pins are on JP2, and
- DE2-70 pins have different names for pins at the same location on the header (e. g., GPIO_0[0] is on JP1-1 of the DE2, but it is on JP1-2 of the DE2-70.

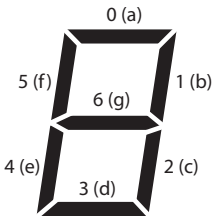

Figure C.1. Naming convention for seven-segment displays. The digit represents the subscript used by the DE2, and the letter represents the most common name used by manufacturers and designers.

Although all pins needed for lab exercises are described here, some that may be needed for final projects may not be included. Refer to the manufacturer's reference manual for the DE2 or DE2-70 board as needed for additional pins.

Table C.1 Pushbutton pin assignments. All switches produce a low signal on the corresponding pin when pressed.

Switch designator	DE2 FPGA pin	DE2-70 FPGA pin
KEY[0]	PIN_G26	PIN_T29
KEY[1]	PIN_N23	PIN_T28
KEY[2]	PIN_P23	PIN_U30
KEY[3]	PIN_W26	PIN_U29

Table C.2 Slide switch pin assignments. All switches produce a low signal on the corresponding pin when in the DOWN position.

Switch	DE2 FPGA pin	DE2-70 FPGA pin
SW[0]	PIN_N25	PIN_AA23
SW[1]	PIN_N26	PIN_AB26
SW[2]	PIN_P25	PIN_AB25
SW[3]	PIN_AE14	PIN_AC27
SW[4]	PIN_AF14	PIN_AC26
SW[5]	PIN_AD13	PIN_AC24
SW[6]	PIN_AC13	PIN_AC23
SW[7]	PIN_C13	PIN_AD25
SW[8]	PIN_B13	PIN_AD24
SW[9]	PIN_A13	PIN_AE27
SW[10]	PIN_N1	PIN_W5
SW[11]	PIN_P1	PIN_V10
SW[12]	PIN_P2	PIN_U9
SW[13]	PIN_T7	PIN_T9
SW[14]	PIN_U3	PIN_L5
SW[15]	PIN_U4	PIN_L4
SW[16]	PIN_V1	PIN_L7
SW[17]	PIN_V2	PIN_L8

Table C.3 LED pin assignments. All LEDs light when corresponding pin is driven high.

LED Designator	DE2 FPGA pin	DE2-70 FPGA pin
LEDR[0]	PIN_AE23	PIN_AJ6
LEDR[1]	PIN_AF23	PIN_AK5
LEDR[2]	PIN_AB21	PIN_AJ5
LEDR[3]	PIN_AC22	PIN_AJ4
LEDR[4]	PIN_AD22	PIN_AK3
LEDR[5]	PIN_AD23	PIN_AH4
LEDR[6]	PIN_AD21	PIN_AJ3
LEDR[7]	PIN_AC21	PIN_AJ2
LEDR[8]	PIN_AA14	PIN_AH3
LEDR[9]	PIN_Y13	PIN_AD14
LEDR[10]	PIN_AA13	PIN_AC13
LEDR[11]	PIN_AC14	PIN_AB13
LEDR[12]	PIN_AD15	PIN_AC12
LEDR[13]	PIN_AE15	PIN_AB12
LEDR[14]	PIN_AF13	PIN_AC11
LEDR[15]	PIN_AE13	PIN_AD9
LEDR[16]	PIN_AE12	PIN_AD8
LEDR[17]	PIN_AD12	PIN_AJ7
LEDG[0]	PIN_AE22	PIN_W27
LEDG[1]	PIN_AF22	PIN_W25
LEDG[2]	PIN_W19	PIN_W23
LEDG[3]	PIN_V18	PIN_Y27
LEDG[4]	PIN_U18	PIN_Y24
LEDG[5]	PIN_U17	PIN_Y23
LEDG[6]	PIN_AA20	PIN_AA27
LEDG[7]	PIN_Y18	PIN_AA24
LEDG[8]	PIN_Y12	PIN_AC14

Table C.4 GPIO 0 (JP1) pin assignments.

	DE2		DE2-70	
Header Pin	**Signal Name**	**FPGA Pin**	**Signal Name**	**FPGA Pin**
JP1-1	GPIO_0[0]	PIN_D25	GPIO_CLKINN0	PIN_T25
JP1-2	GPIO_0[1]	PIN_J22	GPIO_0[0]	PIN_C30
JP1-3	GPIO_0[2]	PIN_E26	GPIO_CLKINP0	PIN_T24
JP1-4	GPIO_0[3]	PIN_E25	GPIO_0[1]	PIN_C29
JP1-5	GPIO_0[4]	PIN_F24	GPIO_0[2]	PIN_E28
JP1-6	GPIO_0[5]	PIN_F23	GPIO_0[3]	PIN_D29
JP1-7	GPIO_0[6]	PIN_J21	GPIO_0[4]	PIN_E27
JP1-8	GPIO_0[7]	PIN_J20	GPIO_0[5]	PIN_D28
JP1-9	GPIO_0[8]	PIN_F25	GPIO_0[6]	PIN_E29
JP1-10	GPIO_0[9]	PIN_F26	GPIO_0[7]	PIN_G25
JP1-11	+5V		+5V	
JP1-12	Ground		Ground	
JP1-13	GPIO_0[10]	PIN_N18	GPIO_0[8]	PIN_E30
JP1-14	GPIO_0[11]	PIN_P18	GPIO_0[9]	PIN_G26
JP1-15	GPIO_0[12]	PIN_G23	GPIO_0[10]	PIN_F29
JP1-16	GPIO_0[13]	PIN_G24	GPIO_0[11]	PIN_G29
JP1-17	GPIO_0[14]	PIN_K22	GPIO_0[12]	PIN_F30
JP1-18	GPIO_0[15]	PIN_G25	GPIO_0[13]	PIN_G30
JP1-19	GPIO_0[16]	PIN_H23	GPIO_CLKOUTN0	PIN_H23
JP1-20	GPIO_0[17]	PIN_H24	GPIO_0[14]	PIN_H29
JP1-21	GPIO_0[18]	PIN_J23	GPIO_CLKOUTP0	PIN_G24
JP1-22	GPIO_0[19]	PIN_J24	GPIO_0[15]	PIN_H30
JP1-23	GPIO_0[20]	PIN_H25	GPIO_0[16]	PIN_J29
JP1-24	GPIO_0[21]	PIN_H26	GPIO_0[17]	PIN_H25
JP1-25	GPIO_0[22]	PIN_H19	GPIO_0[18]	PIN_J30
JP1-26	GPIO_0[23]	PIN_K18	GPIO_0[19]	PIN_H24
JP1-27	GPIO_0[24]	PIN_K19	GPIO_0[20]	PIN_J25
JP1-28	GPIO_0[25]	PIN_K21	GPIO_0[21]	PIN_K24
JP1-29	+3.3V		+3.3V	
JP1-30	Ground		Ground	
JP1-31	GPIO_0[26]	PIN_K23	GPIO_0[22]	PIN_J24
JP1-32	GPIO_0[27]	PIN_K24	GPIO_0[23]	PIN_K25
JP1-33	GPIO_0[28]	PIN_L21	GPIO_0[24]	PIN_L22
JP1-34	GPIO_0[29]	PIN_L20	GPIO_0[25]	PIN_M21
JP1-35	GPIO_0[30]	PIN_J25	GPIO_0[26]	PIN_L21
JP1-36	GPIO_0[31]	PIN_J26	GPIO_0[27]	PIN_M22
JP1-37	GPIO_0[32]	PIN_L23	GPIO_0[28]	PIN_N22
JP1-38	GPIO_0[33]	PIN_L24	GPIO_0[29]	PIN_N25
JP1-39	GPIO_0[34]	PIN_L25	GPIO_0[30]	PIN_N21
JP1-40	GPIO_0[35]	PIN_L19	GPIO_0[31]	PIN_N24

Table C.5 GPIO 1 (JP2) pin assignments.

	DE2		DE2-70	
Header Pin	**Signal Name**	**FPGA Pin**	**Signal Name**	**FPGA Pin**
JP2-1	GPIO_1[0]	PIN_K25	GPIO_CLKINN1	PIN_AH14
JP2-2	GPIO_1[1]	PIN_K26	GPIO_1[0]	PIN_G27
JP2-3	GPIO_1[2]	PIN_M22	GPIO_CLKINP1	PIN_AG15
JP2-4	GPIO_1[3]	PIN_M23	GPIO_1[1]	PIN_G28
JP2-5	GPIO_1[4]	PIN_M19	GPIO_1[2]	PIN_H27
JP2-6	GPIO_1[5]	PIN_M20	GPIO_1[3]	PIN_L24
JP2-7	GPIO_1[6]	PIN_N20	GPIO_1[4]	PIN_H28
JP2-8	GPIO_1[7]	PIN_M21	GPIO_1[5]	PIN_L25
JP2-9	GPIO_1[8]	PIN_M24	GPIO_1[6]	PIN_K27
JP2-10	GPIO_1[9]	PIN_M25	GPIO_1[7]	PIN_L28
JP2-11	+5V		+5V	
JP2-12	Ground		Ground	
JP2-13	GPIO_1[10]	PIN_N24	GPIO_1[8]	PIN_K28
JP2-14	GPIO_1[11]	PIN_P24	GPIO_1[9]	PIN_L27
JP2-15	GPIO_1[12]	PIN_R25	GPIO_1[10]	PIN_K29
JP2-16	GPIO_1[13]	PIN_R24	GPIO_1[11]	PIN_M25
JP2-17	GPIO_1[14]	PIN_R20	GPIO_1[12]	PIN_K30
JP2-18	GPIO_1[15]	PIN_T22	GPIO_1[13]	PIN_M24
JP2-19	GPIO_1[16]	PIN_T23	GPIO_CLKOUTN1	PIN_AF27
JP2-20	GPIO_1[17]	PIN_T24	GPIO_1[14]	PIN_L29
JP2-21	GPIO_1[18]	PIN_T25	GPIO_CLKOUTP1	PIN_AF28
JP2-22	GPIO_1[19]	PIN_T18	GPIO_1[15]	PIN_L30
JP2-23	GPIO_1[20]	PIN_T21	GPIO_1[16]	PIN_P26
JP2-24	GPIO_1[21]	PIN_T20	GPIO_1[17]	PIN_P28
JP2-25	GPIO_1[22]	PIN_U26	GPIO_1[18]	PIN_P25
JP2-26	GPIO_1[23]	PIN_U25	GPIO_1[19]	PIN_P27
JP2-27	GPIO_1[24]	PIN_U23	GPIO_1[20]	PIN_M29
JP2-28	GPIO_1[25]	PIN_U24	GPIO_1[21]	PIN_R26
JP2-29	+3.3V		+3.3V	
JP2-30	Ground		Ground	
JP2-31	GPIO_1[26]	PIN_R19	GPIO_1[22]	PIN_M30
JP2-32	GPIO_1[27]	PIN_T19	GPIO_1[23]	PIN_R27
JP2-33	GPIO_1[28]	PIN_U20	GPIO_1[24]	PIN_P24
JP2-34	GPIO_1[29]	PIN_U21	GPIO_1[25]	PIN_N28
JP2-35	GPIO_1[30]	PIN_V26	GPIO_1[26]	PIN_P23
JP2-36	GPIO_1[31]	PIN_V25	GPIO_1[27]	PIN_N29
JP2-37	GPIO_1[32]	PIN_V24	GPIO_1[28]	PIN_R23
JP2-38	GPIO_1[33]	PIN_V23	GPIO_1[29]	PIN_P29
JP2-39	GPIO_1[34]	PIN_W25	GPIO_1[30]	PIN_R22
JP2-40	GPIO_1[35]	PIN_W23	GPIO_1[31]	PIN_P30

Table C.6 Seven-segment display pin assignments, digits HEX0-HEX3. All segments light when corresponding pin is driven low.

Segment Designator	DE2 FPGA pin	DE2-70 FPGA pin
HEX0[0]	PIN_AF10	PIN_AE8
HEX0[1]	PIN_AB12	PIN_AF9
HEX0[2]	PIN_AC12	PIN_AH9
HEX0[3]	PIN_AD11	PIN_AD10
HEX0[4]	PIN_AE11	PIN_AF10
HEX0[5]	PIN_V14	PIN_AD11
HEX0[6]	PIN_V13	PIN_AD12
HEX0_DP		PIN_AF12
HEX1[0]	PIN_V20	PIN_AG13
HEX1[1]	PIN_V21	PIN_AE16
HEX1[2]	PIN_W21	PIN_AF16
HEX1[3]	PIN_Y22	PIN_AG16
HEX1[4]	PIN_AA24	PIN_AE17
HEX1[5]	PIN_AA23	PIN_AF17
HEX1[6]	PIN_AB24	PIN_AD17
HEX1_DP		PIN_AC17
HEX2[0]	PIN_AB23	PIN_AE7
HEX2[1]	PIN_V22	PIN_AF7
HEX2[2]	PIN_AC25	PIN_AH5
HEX2[3]	PIN_AC26	PIN_AG4
HEX2[4]	PIN_AB26	PIN_AB18
HEX2[5]	PIN_AB25	PIN_AB19
HEX2[6]	PIN_Y24	PIN_AE19
HEX2_DP		PIN_AC19
HEX3[0]	PIN_Y23	PIN_P6
HEX3[1]	PIN_AA25	PIN_P4
HEX3[2]	PIN_AA26	PIN_N10
HEX3[3]	PIN_Y26	PIN_N7
HEX3[4]	PIN_Y25	PIN_M8
HEX3[5]	PIN_U22	PIN_M7
HEX3[6]	PIN_W24	PIN_M6
HEX3_DP		PIN_M4

Table C.7 Seven-segment display pin assignments, digits HEX4-HEX7. All segments light when corresponding pin is driven low.

Segment Designator	DE2 FPGA pin	DE2-70 FPGA pin
HEX4[0]	PIN_U9	PIN_P1
HEX4[1]	PIN_U1	PIN_P2
HEX4[2]	PIN_U2	PIN_P3
HEX4[3]	PIN_T4	PIN_N2
HEX4[4]	PIN_R7	PIN_N3
HEX4[5]	PIN_R6	PIN_M1
HEX4[6]	PIN_T3	PIN_M2
HEX4_DP		PIN_L6
HEX5[0]	PIN_T2	PIN_M3
HEX5[1]	PIN_P6	PIN_L1
HEX5[2]	PIN_P7	PIN_L2
HEX5[3]	PIN_T9	PIN_L3
HEX5[4]	PIN_R5	PIN_K1
HEX5[5]	PIN_R4	PIN_K4
HEX5[6]	PIN_R3	PIN_K5
HEX5_DP		PIN_K6
HEX6[0]	PIN_R2	PIN_H6
HEX6[1]	PIN_P4	PIN_H4
HEX6[2]	PIN_P3	PIN_H7
HEX6[3]	PIN_M2	PIN_H8
HEX6[4]	PIN_M3	PIN_G4
HEX6[5]	PIN_M5	PIN_F4
HEX6[6]	PIN_M4	PIN_E4
HEX6_DP		PIN_K2
HEX7[0]	PIN_L3	PIN_K3
HEX7[1]	PIN_L2	PIN_J1
HEX7[2]	PIN_L9	PIN_J2
HEX7[3]	PIN_L6	PIN_H1
HEX7[4]	PIN_L7	PIN_H2
HEX7[5]	PIN_P9	PIN_H3
HEX7[6]	PIN_N9	PIN_G1
HEX7_DP		PIN_G2

Table C.8 VGA interface pin assignments.

Function	Signal name	DE2 FPGA pin	DE2-70 FPGA pin
VGA Red[0]	VGA_R[0]	PIN_C8	PIN_D23
VGA Red[1]	VGA_R[1]	PIN_F10	PIN_E23
VGA Red[2]	VGA_R[2]	PIN_G10	PIN_E22
VGA Red[3]	VGA_R[3]	PIN_D9	PIN_D22
VGA Red[4]	VGA_R[4]	PIN_C9	PIN_H21
VGA Red[5]	VGA_R[5]	PIN_A8	PIN_G21
VGA Red[6]	VGA_R[6]	PIN_H11	PIN_H20
VGA Red[7]	VGA_R[7]	PIN_H12	PIN_F20
VGA Red[8]	VGA_R[8]	PIN_F11	PIN_E20
VGA Red[9]	VGA_R[9]	PIN_E10	PIN_G20
VGA Green[0]	VGA_G[0]	PIN_B9	PIN_A10
VGA Green[1]	VGA_G[1]	PIN_A9	PIN_B11
VGA Green[2]	VGA_G[2]	PIN_C10	PIN_A11
VGA Green[3]	VGA_G[3]	PIN_D10	PIN_C12
VGA Green[4]	VGA_G[4]	PIN_B10	PIN_B12
VGA Green[5]	VGA_G[5]	PIN_A10	PIN_A12
VGA Green[6]	VGA_G[6]	PIN_G11	PIN_C13
VGA Green[7]	VGA_G[7]	PIN_D11	PIN_B13
VGA Green[8]	VGA_G[8]	PIN_E12	PIN_B14
VGA Green[9]	VGA_G[9]	PIN_D12	PIN_A14
VGA Blue[0]	VGA_B[0]	PIN_J13	PIN_B16
VGA Blue[1]	VGA_B[1]	PIN_J14	PIN_C16
VGA Blue[2]	VGA_B[2]	PIN_F12	PIN_A17
VGA Blue[3]	VGA_B[3]	PIN_G12	PIN_B17
VGA Blue[4]	VGA_B[4]	PIN_J10	PIN_C18
VGA Blue[5]	VGA_B[5]	PIN_J11	PIN_B18
VGA Blue[6]	VGA_B[6]	PIN_C11	PIN_B19
VGA Blue[7]	VGA_B[7]	PIN_B11	PIN_A19
VGA Blue[8]	VGA_B[8]	PIN_C12	PIN_C19
VGA Blue[9]	VGA_B[9]	PIN_B12	PIN_D19
VGA Clock	VGA_CLK	PIN_B8	PIN_D24
VGA BLANK	VGA_BLANK	PIN_D6	PIN_C15
VGA H_SYNC	VGA_HS	PIN_A7	PIN_J19
VGA V_SYNC	VGA_VS	PIN_D8	PIN_H19

Table C.9 Miscellaneous pin assignments.

Function	Signal name	DE2 FPGA pin	DE2-70 FPGA pin
27 MHz clock	CLOCK_27	PIN_D13	
28 MHz clock	CLOCK_28		PIN_E16
50 MHz clock	CLOCK_50	PIN_N2	PIN_AD15
50 MHz clock	CLOCK_50_2		PIN_D16
50 MHz clock	CLOCK_50_3		PIN_R28
50 MHz clock	CLOCK_50_4		PIN_R3
External clock (SMA)	EXT_CLOCK	PIN_P26	PIN_R29
PS/2 Clock	PS2_CLK	PIN_D26	PIN_F24
PS/2 Data	PS2_DAT	PIN_C24	PIN_E24